circuit is equal to a power supply voltage applied to the second MOS transistors constituting the internal circuit.

4. (Amended) A semiconductor device according to Claim 2, wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors.

7. (Amended) A semiconductor device according to Claim 1, wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is higher than a power supply voltage applied to the second MOS transistors constituting the internal circuit.

Please add the following claims:

21. (New) A semiconductor device according to Claim 2, wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is equal to a power supply voltage applied to the second MOS transistors constituting the internal circuit.

22. (New) A semiconductor device according to Claim 21, wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors.

23. (New) A semiconductor device according to Claim 3, wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors.

24. (New) A semiconductor device according to Claim 21, wherein a gate insulating film thickness of the first MOS transistors is equal to a gate insulating film thickness of the second MOS transistors.

25. (New) A semiconductor device according to Claim 21, wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.

26. (New) A semiconductor device according to Claim 2, wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is higher than a power supply voltage applied to the second MOS transistors constituting the internal circuit.